REMARKS

The application contains claims 3-7, 9-12, 17-20, 23, and 25-26. By this amendment, claims 1, 21, and 22 have been canceled. In view of the foregoing amendments and following remarks, Applicants respectfully request allowance of the application.

INTERVIEW SUMMARY

Applicants thank the Examiner for the courtesy extended during the personal interview conducted on April 20, 2004. During the interview, the rejections to all independent claims were discussed. The Examiner has agreed that claim 4 is allowable over Pickett and Henessy. With regards to other independent claims, no agreement was reached.

CLAIM OBJECTIONS

Applicants believe that the foregoing amendments overcome all claim objections noted in paragraphs 3-7 of the Final Office Action and Advisory Action.

PRIOR ART REJECTIONS

All pending claims stand rejected based on prior art. Applicants respectfully request withdrawal of these outstanding rejections because the prior art does not disclose, teach, or suggest all elements of the pending claims.

Claims 4-6 are allowable over the cited art.

Claim 4 stands rejected as obvious over Pickett (U.S. Patent No. 5,968,169) and Hennessy. As discussed during the interview, the hypothesis provided in the Office Action conflicts with express disclosure from Pickett. The Office Action surmised that stalling would be required if multiple calls were issued by Pickett's decoding units. Actually, Pickett's pipelines are prioritized; if multiple calls were issued simultaneously to his stack, the call from the highest priority decoding unit 208 would succeed and the other calls would be ***discarded*** (col. 12, lines 50-67). Pickett, therefore, teaches against stalling as recited in claim 4.

Hennessy does not cure this deficiency of Pickett. Hennessy discloses the various structural hazards in the context of a general system memory, but they do not involve a return stack buffer. Additionally, Hennessy mentions anything about two call instructions competing for the same location with the return stack buffer, anything about a call instruction with a predetermined access rate to a return stack buffer, or any of these events alleged by the Examiner. Accordingly, the obviousness rejection to claim 4 must be withdrawn. Claims 5-6, which depend from independent claim 4, also define over the cited art.

Claims 7 and 9 are allowable over the cited art.

Claims 7 and 9 stand rejected as obvious over Hennessy and Hoyt (U.S. Patent No. 5,604,877). Claim 7 has been amended and now recites:

> determining, with reference to other call and/or return instructions read previously from the instruction pipestage, whether immediate processing of the call instruction would exceed the instruction pipe's access allocation to the return stack buffer.

None of the cited art discloses, teaches, or suggests determining whether immediate processing of the call instruction would exceed the instruction pipe's access allocation to a return stack buffer. Hennessy discloses various structural hazards, but they do not involve either call instructions or a return stack buffer. Instead, they involve only general memory. In Hoyt, only one pipeline is accessing a return stack buffer, and thus, Hoyt's pipe has a 100% access rate to the return stack buffer. Thus, there is no need to allocate the instruction pipe's access to the external source. Therefore, the alleged combination of Hennessy and Hoyt fails to render claim 7 obvious. Accordingly, claims 7 and 9 define over the art.

Claims 10-12 are allowable over the prior art.

Claims 10-12 stand rejected as anticipated by the IBM TB. Claim 10 recites in part:

> if the return address is available immediately upon receipt of the return instruction at the instruction pipe stage, forwarding the return address to a next pipe state during a next clock cycle,
>
> if not, stalling processing of the return instruction until the round-trip communication latency period expires and forwarding a received return address thereafter

The IBM TB does not teach or suggest this claimed feature. There is no staggered timing relationship in the IBM system as recited in the claims – no "slow" or "fast" delivery of return addresses. Accordingly, the anticipation rejection of independent claim 10 should be withdrawn. Claims 11-12, which depend from claim 10, also define over the art.

Claims 17-20 are allowable over the prior art.

Claims 17-20 stand rejected as obvious over Pickett and Sproch et al. (U.S. Patent No. 6,247,134). Claim 17 recites:

> a return-stack buffer coupled to the first instruction pipe and the second instruction pipe by communication paths of differing communication latencies.

Pickett does not disclose, teach, or suggest this claimed feature. Pickett's decoder units appear to communicate with its stack via communication paths that have common communication latencies. See Pickett, FIGs. 1 and 2. Sproch's system only includes one pipeline. Thus, independent claim 17 is patentable over the cited art. Accordingly, claims 18-20, which depend from claim 17, are also patentable over the art.

Claim 23 is allowable over the prior art.

Claim 23 stands rejected as anticipated by Hoyt. Claim 24 stands rejected as obvious over Hoyt and the IBM TB. Claim 23 has been amended to recite:

> responsive to a return instruction in a first pipestage of an instruction pipe:
> determining whether the pipestage processed a prior return instruction faster than a latency period for round trip communication between the pipestage and the return stack buffer,
> if so, stalling the downstream pipestages until the period for processing a prior return instruction equals the round trip communication latency period

As indicated by the Examiner, Hoyt does not teach this subject matter. The IBM TB fails to cure the deficiency of Hoyt. The IBM TB discloses that "if a return is followed by another return instruction **before the first one completes**, you need to hold the second return in decode until the first one completes in write back stage." This "before the first one completes" refers to execution time of a return instruction (or the time it takes to execute a return instruction), but not the round-trip communication latency period with the return stack buffer. Thus, the IBM TB fails to disclose, teach, or suggest stalling the pipestages until the period for processing

a prior return instruction equals the round trip communication latency period. Hoyt also mentions nothing about the round-trip communication latency period. Thus, even the alleged combination of these two references falls short of disclosing this claimed feature. Accordingly, claim 23 defines over the art.

Claims 25-26 are allowable over the prior art.

Claims 25-26 stand rejected as obvious over Hoyt and Cosgrove et al. (U.S. Patent No. 4,399,507). Claim 25 recites in part:

> a pair of registers provided between first and second pipestages of the plurality,
> a first of the registers to store a return address received from the first pipestage during receipt of a call instruction,
> a second of the registers to store a return address received from a return stack buffer.

Neither Hoyt nor Cosgrove disclose, teach, or suggest a pair of local storage devices, one receiving a return instruction from within the instruction pipe and the other receiving an instruction from a return stack buffer. The Examiner alleges that it would be obvious to modify Hoyt to include a second register as taught by Cosgrove to allow quick address access for a next instruction. The Examiner's assertion is based on Hoyt's disclosure of a return register, which stores a predicted return address before storing the address in the return stack buffer and Cosgrove' disclosure of a register, which stores a return address received from a return stack buffer. But, there is nothing in Hoyt or Cosgrove that provides any suggestion or motivation to combine these two registers. In fact, both Hoyt and Cosgrove disclose a system with only one register. Further, the Examiner fails to give any plausible reason or cite any reference that would motivate or even suggest to one skilled in the art at the time of the invention to combine Hoyt and Cosgrove to include two registers; one to store a return address from a return stack buffer and the other to store a return address from an instruction pipe, as claimed in claim 25. Again, the references themselves or some other teaching must provide some suggestion or motivation to combine their teachings. The Examiner may not conclude that Applicants' invention is obvious based on improper hindsight reasoning. Accordingly, claim 25 and its dependent claim 26 define over the art.

CONCLUSION

In view of the above amendments and remarks, Applicants respectfully submit that the present application is now in condition for allowance. A timely Notice to that effect is earnestly solicited. The Examiner is invited to contact the undersigned at (202) 220-4200 to discuss any aspect of the application.

Respectfully submitted,

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